Claims 2, 4, 5, 8, 12 and 13 have been amended, as shown on the attached sheet, to overcome the Examiner's objection. Thus, withdrawal of the rejection of claims 2, 4, 5, 8, 12 and 13 under 35 U.S.C. §112, second paragraph is respectfully requested.

Claims 4 and 12 were rejected under 35 U.S.C. §112, first paragraph as containing subject matter which was not described in the specification in such as way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the invention.

Claims 4 and 12 have been further amended, as shown on the attached sheet, to overcome this rejection. Therefore, withdrawal of the rejection of claims 4 and 12 under 35 U.S.C. §112, first paragraph is respectfully requested.

Claims 1-16 were rejected under 35 U.S.C. §103(a) as being unpatentable over Maruyama et al. (U.S. Patent No. 2001/0003199 A1) in view of Dye (U.S. Patent No. 6,173,381 B1). With respect to claims 1, 4, 7 and 12 the Examiner states that Maruyama et al. discloses all of the features recited in claims 1, 4, 7 and 12 except for the use of two address conversion units to assign physical addresses of the first and the second memory units to their respective logical addresses. However, the Examiner states that Dye teaches the use of two address conversion units to control different banks of memory unit, and that it would have been obvious to one of ordinary skill in the art to modify the microprocessor of Maruyama to have two separate address conversion units as taught by Dye, in order to be able to address a large amount of memory that may be required for image processing.

This rejection is respectfully traversed, because the combination of Maruyama et al. and Dye fails to disclose, teach or suggest all the features recited in the rejected claims.

For example, claim 1 recites a microprocessor to which a plurality of memory units having physical addresses different from each other are externally connected, with the microprocessor comprising a first address conversion unit which assigns a physical address of a first memory unit out of the plurality of memory units to a logical address of a load module stored in the first memory unit, wherein the load module includes instructions and data. Claim 1 also recites a copying unit which copies an instruction code from the load module stored in the first memory unit to a second memory unit out of the plurality of memory units and a second address conversion unit which assigns a physical address of the second memory unit to a logical address of the instruction code copied to the second memory unit.

First, as admitted by the Examiner and discussed above, Maruyama et al. fails to disclose, teach or suggest at least the first and second address conversion units which assign physical addresses as recited in claim 1. Bye fails to remedy this deficiency, because Bye merely discloses that two IMCs (memory controllers) 140a and 140b are coupled between the host/PCI/Cache bridge 105 and the system memory 110. Bye discloses that the IMC 140a is used solely for memory control functions and the IMC 140b is used solely for graphical and audio functions. Alternately, the IMCs 140a and 140b each perform both memory and graphics/audio functions for increased performance (Column 10, lines 33-43).

However, there is no teaching or suggestion in Bye that the IMCs 140a and 140b assign a physical addresses of memory units as recited in claim 1 of the current invention. The IMCs of Bye are not equivalent to the address conversion units recited in claim 1.

Secondly, the combination of Maruyama et al. and Dye fails to disclose, teach or suggest the feature of a first address conversion unit which assigns a physical address of a first memory unit out of said plurality of memories to a logical address of a load module stored in said first memory unit, wherein said load module includes instructions and data and a copying unit which copies an instruction code from said load module stored in said first memory unit to a second memory unit out of said plurality of memory units as recited in claim 1.

In the current invention, the first memory unit (the main memory) is comprised of a memory of a large capacity such as a DIMM (a dual inline memory module). The second memory unit (the local memory) is a memory which is smaller in capacity than the first memory unit (the main memory) but is operated at a higher speed as recited in claims 10, 15, 17 and 18 and described in the Specification page 5, lines 14-19.

Accordingly, when the microprocessor executes an instruction, it gets the instruction code from the high-speed second memory unit (the local memory). Then, the microprocessor executes the instruction. Also, the instruction code is generally high in the locality. Therefore, even if the second memory unit (the local memory) is a memory of a small capacity, a higher speed can be sufficiently produced (Specification page 5, line 20-Page 6, line 2).

However, the large-scale data used in image processing or the like is generally low in locality. Therefore, even if such data is allocated and transferred to the small-capacity second memory unit (the local memory), a higher speed cannot be sufficiently produced do to a loss caused by frequent transferring. Thus, as recited in claim 1 of the current invention, the entire load module including data as well as the instruction codes are stored in the large capacity first memory unit (the main memory), while only the instruction codes of the load module are stored in the second memory unit (Specification page 6, lines 3-10).

Maruyama et al. does not disclose the different uses of a first and second memory as recited in claim 1 and discussed above. In fact, Maruyama contrarily discloses a ROM 12 equivalent to a first memory in which the program has been recorded, the RAM 14 equivalent to a second memory operating higher in speed than the ROM 12 so that the same program developed in different physical addresses in different memories can be executed by setting the program space 6 for use in executing a virtual program beforehand in the memory space 5 of the CPU 11 in order to alter the address of the program space 6 for which translation is intended. Consequently, the program is executed by selecting the ROM 12 when it is desirable to secure a wide working area and the RAM 14 is releasable from being reserved as a programmable memory. When the RAM 14 has a sufficient capacity, on the other hand, the print processing program 22 of the ROM 12 is developed in the RAM 14 capable of exchanging data with the CPU 11 at high speed so as to improve the program executing speed (Page 4 Column 1, paragraph [0047] - Column 2, paragraph [00048]).

Consequently, Maruyama et al. merely discloses that the address translating destination of the program space is allocated to one of the memories according to whether there is space left in the second memory. Thus, Maruyama et al. does not teach or suggest the separate uses of the first and second memories as recited in claim 1 of the current invention.

Bye fails to remedy these deficiencies of Maruyama et al. because it is merely directed to a memory controller (IMC) which includes data compression/decompression engines for improved performance. The memory controller (IMC) sits on the main CPU bus or a high speed system peripheral bus such as a PCI bus and includes one or more symmetric memory ports for connecting to system memory as well as video outputs to directly drive a video display monitor (Column 2, lines 34-45).

Consequently, claim 1 is patentable over the combination of Maruyama et al. and Bye. Independent claims 4, 7 and 12 also recite the above features of claim 1. Claims 4, 7 and 12 recite first and second address conversion units which assign physical addresses. Claims 4, 7 and 12 also recite assigning a physical address of a first memory unit out of the plurality of memory units to a logical address of a load module stored in said first memory unit, wherein said load module includes instructions and data and a copying unit which copies an instruction code from said load module stored in said first memory unit to a second memory unit out of said plurality of memory units as recited in claim 1.

Therefore, claims 4, 7 and 12 are patentable for at least the same reasons discussed above with respect to claim 1.

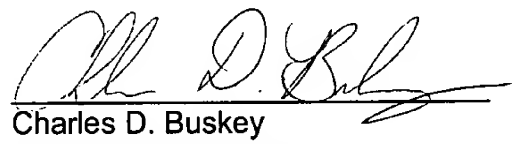
Moreover, claims 2-3, 5-6, 8-11 and 13-16 depend from claims 1, 4, 7 and 12 respectively. Therefore, claims 2-3, 5-6, 8-11 and 13-16 are patentable for at least the reasons discussed above with respect to claims 1, 4, 7 and 12.

Thus, for the above reasons, withdrawal of the rejection of claims 1-16 under 35 U.S.C. §103(a) over Maruyama et al. in view of Dye is respectfully requested.

If for any reason, the Examiner determines that the application is not in condition for allowance, it is respectfully requested that the Examiner contact by telephone, the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the Applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension, together with any additional fees, may be charged to counsel's Deposit Account Number 01-2300 making reference to Attorney Docket No. 108391-00011.

Respectfully submitted,



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Enclosure: Marked-Up Copy of Claims

## MARKED-UP COPY OF THE CLAIMS

1. (Amended) A microprocessor to which a plurality of memory units having physical addresses different from each other are externally connected, said microprocessor comprising:

a first address conversion unit which assigns a physical address of a first memory unit out of said plurality of memory units to a logical address of a load module stored in said first memory unit, wherein said load module includes instructions and data;

a copying unit which copies an instruction code from said load module stored in said first memory unit to a second memory unit out of said plurality of memory units; and

a second address conversion unit which assigns a physical address of said second memory unit to a logical address of the instruction code copied to said second memory unit.

2. (Amended) The microprocessor according to claim 1, wherein when said load module stored in said [second] first memory unit is accessed, said first address conversion unit assigns the physical address of said first memory unit to the logical address of said load module to be accessed, and said second address conversion unit assigns the physical address of said second memory unit to said logical address of the instruction code from said load module to be accessed.

4. (Amended) A microprocessor to which a plurality of memory units having physical addresses different from each other are externally connected, said microprocessor comprising:

a first address conversion unit which assigns a physical address of a first memory unit out of said plurality of memory units to a logical address of a load module stored in said first memory unit, wherein said load module includes instructions and data;

a [storage] processing unit which temporarily stores and copies an instruction code from said load module stored in said first memory unit to a second memory unit out of said plurality of memory units; and

a second address conversion unit which assigns a physical address of said second memory unit to a logical address of the instruction code stored in said second memory unit.

5. (Amended) The microprocessor according to claim 4, wherein when said load module stored in said [second] first memory unit is accessed, said first address conversion unit assigns the physical address of said first memory unit to the logical address of said load module to be accessed, and said second address conversion unit assigns the physical address of said second memory unit to said logical address of the instruction code from said load module to be accessed.

7. (Amended) A memory device comprising:

a plurality of memory units having physical addresses different from each other;

a first address conversion unit which assigns a physical address of a first memory unit out of said plurality of memories to a logical address of a load module stored in said first memory unit, wherein said load module includes instructions and data;

a copying unit which copies an instruction code from said load module stored in said first memory unit to a second memory unit out of said plurality of memory units; and

a second address conversion unit which assigns a physical address of said second memory unit to a logical address of the instruction code copied to said second memory unit.

8. (Amended) The memory device according to claim 7, wherein when said load module stored in said [second] first memory unit is accessed, said first address conversion unit assigns the physical address of said first memory unit to the logical address of said load module to be accessed, and said second address conversion unit assigns the physical address of said second memory unit to said logical address of the instruction code from said load module to be accessed.

12. (Amended) A memory device comprising:

a plurality of memory units having physical addresses different from each other;

a first address conversion unit which assigns a physical address of a first memory unit out of said plurality of memory units to a logical address of a load module stored in said first memory unit, wherein said load module includes instructions and data;

a [storage] processing unit means which temporarily stores and copies an instruction code from said load module stored in said first memory unit to a second memory unit out of said plurality of memory units; and

a second address conversion unit which assigns a physical address of said second memory unit to a logical address of the instruction code stored in said second memory unit.

13. (Amended) The memory device according to claim 12, wherein when said load module stored in said [second] first memory unit is accessed, said first address conversion unit assigns the physical address of said first memory unit to the logical address of said load module to be accessed, and said second address conversion unit assigns the physical address of said second memory unit to said logical address of the instruction code from said load module to be accessed.